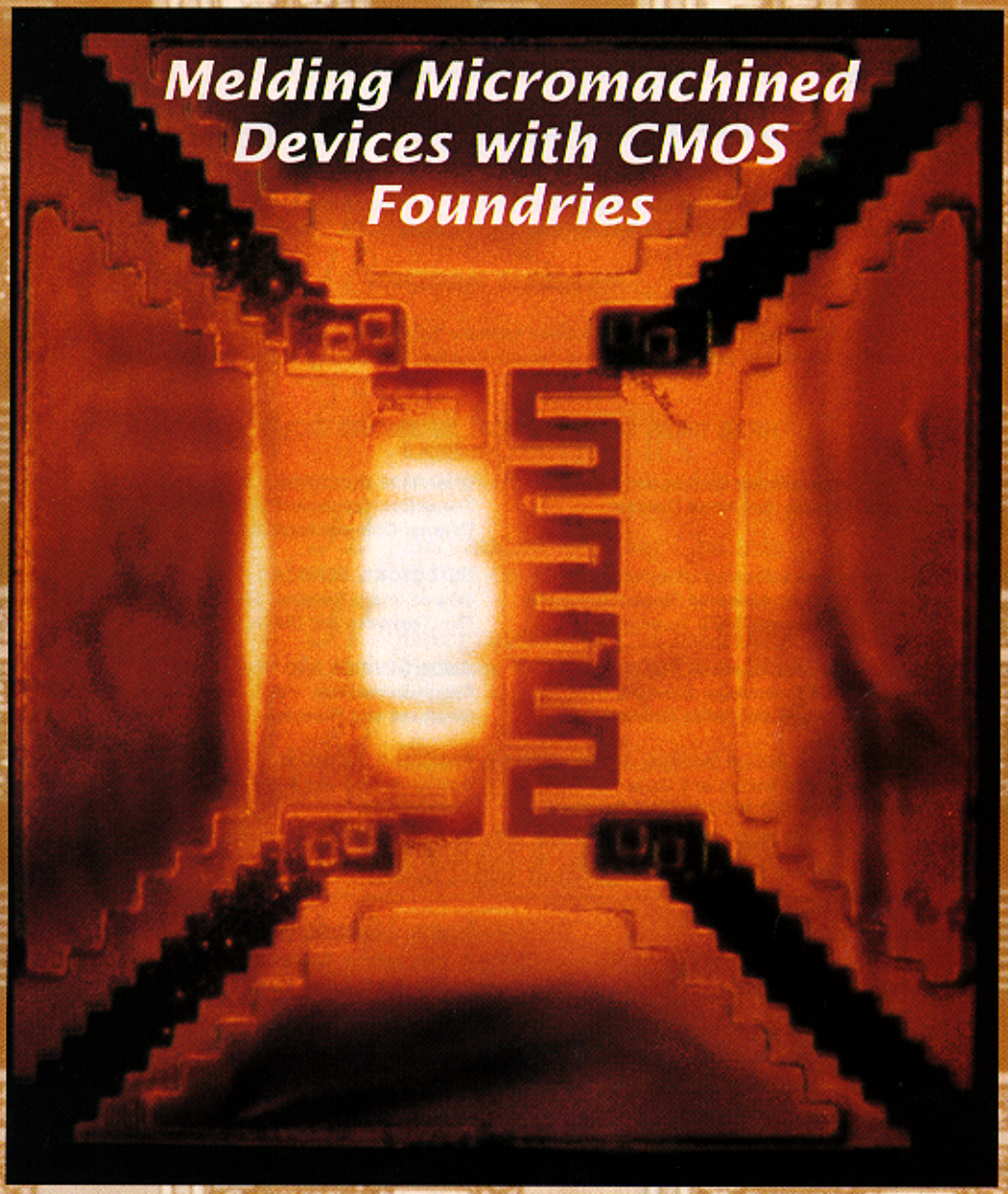
Vol. 8, No. 6 ■ November 1992

IEEE Circuits & Devices

THE MAGAZINE OF ELECTRONIC AND PHOTONIC SYSTEMS



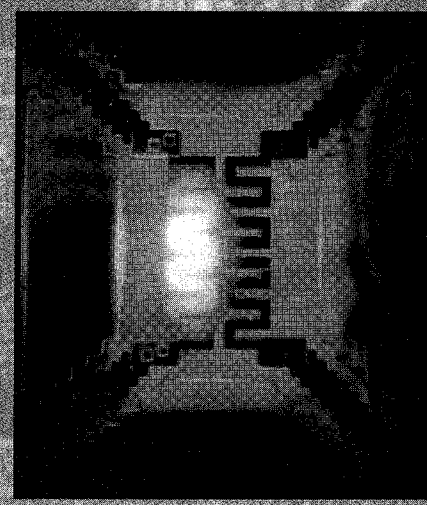
Melding Micromachined Devices with CMOS Foundries

In this issue:

- Flip-Chip Bonding Optimizes OEICs
- Bipolar Circuits Beyond ECL
- Optical Interconnects Pick Up Speed
- Fast CMOS Gets Out of the Cold
- IEDM Pre-Conference Coverage

by Janet C. Marshall, M. Parameswaran,
Mona E. Zaghloul, and Michael Gaitan

High-Level CAD Melds Micromachined Devices with Foundries



Cost-effective silicon micromachined devices can be fabricated in a standard CMOS foundry through the MOSIS service

Standard commercial CMOS foundries have now been successfully used for the fabrication of silicon micromachined devices [1-4]. To support the routine use of CMOS foundries for micromachining, we need high-level computer-aided-design (CAD) software such as Magic* for device design and integration with digital and analog electronics [5,6].

Magic can generate a CIF (Caltech Intermediate Form) or calma file that contains the mask-specific digitized data. This file can be sent to MOSIS. Manufacturing micromachined structures with standard foundry processes such as those available through the MOSIS service [7] can produce many benefits. These include low cost, high yield, and easy integration of digital and analog electronics with the reliability of a standard process automatically

*This article identifies commercial equipment, instruments, and computer programs to specify procedures adequately. This identification does not imply recommendation or endorsement by NIST, nor does it imply that the identified equipment or program is the best available for the purpose.

Table 1: Magic Section Keywords

Section Keyword	Description
tech	technology file name
planes	listing of the planes
types	listing of the tiles associated with which planes
contact	contacts between planes
styles	colors associated with the tiles
compose	to create structures in the same plane
cifoutput	to output a CIF or calma file
cifinput	to read in a CIF or calma file
drc	design rule checker

built into the circuit. Standard foundries also make silicon micromachining possible for universities, government laboratories, and businesses that do not have an in-house custom integrated circuit (IC) fabrication facility.

In this article, we will describe using the Magic technology file to build transducer devices in the form of micro-heaters for use as IR pixels in a thermal display. Most of the smart microelectronic transducers reported to date consist of substrate electronics with one or more additional specialized layers of polysilicon, piezoelectric, or pyroelectric material. The substrate electronics implements the drive and control functions, while the additional layer(s) produce the transducer function.

The transducer function is based on the material properties of the additional layer(s). The concept of integrating the transducer device on the same substrate as the drive and control electronics, instead of attaching it mechanically, is highly desirable and leads to lower-cost systems (when the systems are produced in high volume). This is equivalent to the savings realized from VLSI circuits as opposed to expensive printed circuit boards containing discrete devices. This concept is generally referred to as integration; transducers that are integrated with substrate electronics are called smart transducers [8].

When smart transducers are manufactured, the circuitry is usually fabricated first with a standard IC fabrication process. After the circuits are fabricated, the transducers are realized with additional post-processing steps. These steps can include the deposition and etching of specialized layers of polysilicon, piezoelectric, or pyroelectric material, as well as the micromachining of silicon. Post-processing steps usually create suspended structures such as diaphragms and cantilevers by removing a sacrificial material [9] or by micromachining a portion of the silicon substrate [10,11]. These are usually custom steps that require specialized processing tools.

High-level CAD software is needed to design these structures into large systems without excessive complexity and design time [12]. In this work, a design methodology is presented that was incorporated into the current MOSIS SCMOS technology file for Magic to implement the fabrication of silicon micromachined device structures. This technology file uses only the layers supplied by a commercial standard CMOS process. Currently-available higher-level CAD editors need modifications before they can be used for the automated design of micromachined devices.

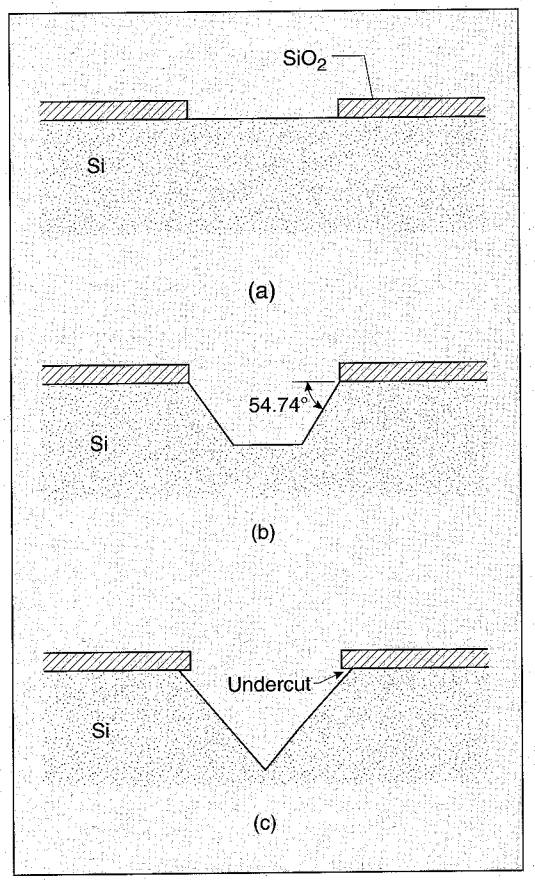
Technology files for Magic contain technology-specific information such as mask layers and design rules. In order to incorporate a new layer called "open" that exposes the appropriate area for an anisotropic etch, we had to modify the technology file. It is this modification of the SCMOS technology file that makes micromachining through MOSIS possible.

The main advantages of this technique is that no major equipment is needed and the post-processing is reduced to a single, maskless etch step. The main disadvantage is that custom layers can not be incorporated into the design; therefore, the sensors/transducers can only be composed of polysilicon and/or aluminum sandwiched with thermal oxide and CVD oxide. The resulting suspended structures have a very low thermal mass and can be heated to incandescence with low power, characteristics that have already permitted these structures to be used as gas flow sensors [2] and micro-heaters for infrared point sources [3].

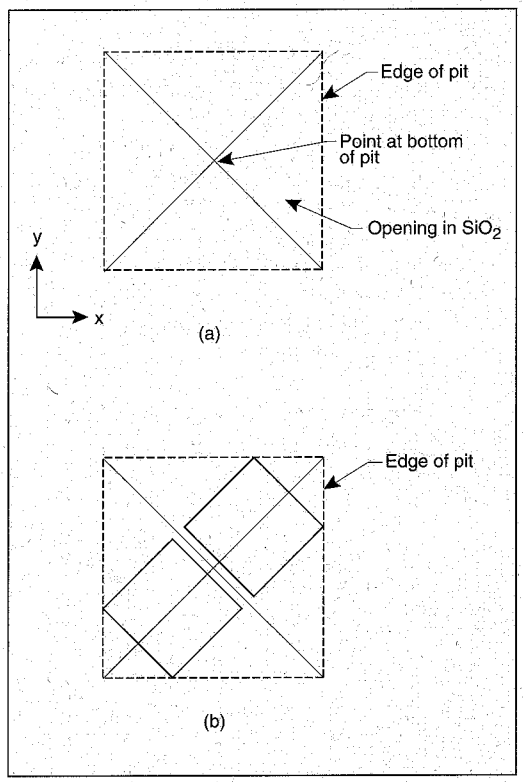
Magic Technology File

The Magic technology file [5,6] is composed of sections, each starting with a keyword and ending with the word "end," as shown below:

"section keyword"
.
.
.
end



1. The effect of an anisotropic etchant on an exposed silicon substrate before the etchant is applied (a), at an intermediate stage (b), and when the etching has stopped (c).



2. When open areas are misaligned with the x-y grid system for a single opening (a), the etched pit will be formed by the smallest rectangle aligned to the x-y grid that encompasses the open region (b), and for two open areas with intersecting pit regions, the etched pit becomes the smallest rectangular area formed by the two openings combined.

A listing of some of the Magic section "keywords" that appear in this article are shown in Table I. Each section of a technology file consists of a series of lines, and each line consists of a series of words separated by spaces.

The "tech" section defines the technology to be used, and the "planes" section specifies the names of the planes to be used. The "types" section identifies the technology-specific tiles used by Magic and the plane on which they reside. Each tile can be categorized as a primary layer, an interconnection between layers, or a transistor. No two tiles on the same plane can reside on the same digitized space. If this is attempted, either a new tile is created or the previous tile is erased. Each line in the "types" section is in the form of *"plane names(tiles)."*

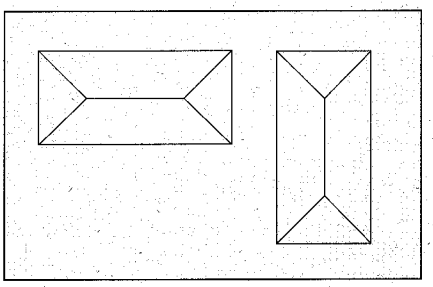
The "styles" section lists all the tiles along with the color-coded numbers used to make up each tile on the CAD system. The "cifoutput" section describes how to generate mask layers from Magic's abstract layers. The mask layers are indicated by the CIF names, which consist of three capital letters starting with the letter C (for CMOS). The two following letters specify the intended mask. In the "cifoutput" section, the CIF names are followed by the Magic tile names to be included on the mask associated with the CIF name. The "cifinput" section defines the operation(s) needed to rebuild a Magic file from a CIF file of digitized mask data. Each Magic tile is specified first, followed by a combination of CIF layers. The "drc" section specifies the design rules, e.g., the width and spacing for the various tiles.

Micromachining in the Technology File

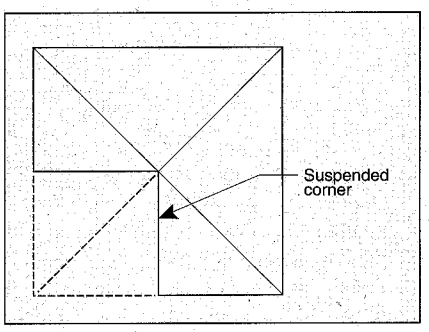
To permit the design of micromachined silicon devices using standard CMOS processes, we modified Magic's technology file to define a new tile and plane called "open." (See Appendix.) The new "open" tile makes micromachining through MOSIS possible. The modified "tech" section calls the new technology file "scm," an abbreviation for scalable CMOS micromachine. The addition of the new "open" plane to the "planes" section results in a total of seven planes, some of which are referred to by more than one name. The scm technology file lists 23 tiles in the "types" section, each of which resides on one of the seven planes. A new line is added to "styles" section to include the new CAD color code for the tile "open."

In the "cifoutput" section, the open area is specified on four different masks. Whenever the open area is digitized on the CAD system and CIFed, the digitized area will be included on the active-area mask (CAA), the contact mask (CCA), the via mask (CVA), and the glass mask (COG). These are the mask steps that will expose the silicon surface during the fabrication process. In practice, after the chips are received from the foundry through MOSIS, the suspended machined devices are realized by performing an additional maskless etch in EDP (ethylene diamine-pyrocatechol-water). In this work, the EDP etchant was purchased premixed from the Transene Company, Inc., part number PSE-300. The etch solution reacts with the exposed silicon surface defined by the digitized open areas, while the SiO_2 acts as a mask [10,11].

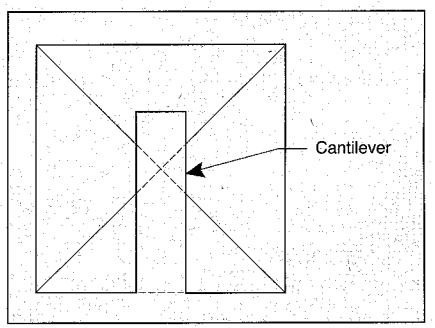
In the "cifinput" section, the layer "open" is defined as any tile containing the



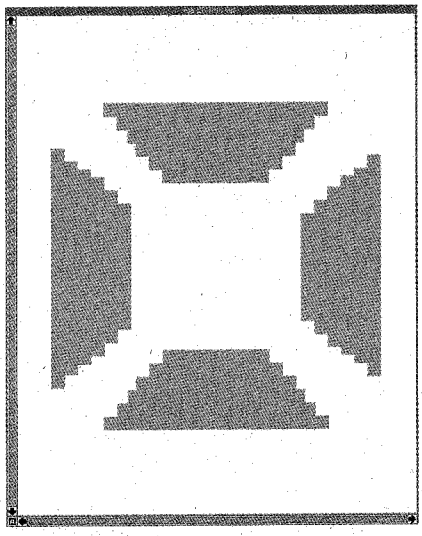
3. Top view of two openings that are isolated and aligned with the x-y grid.



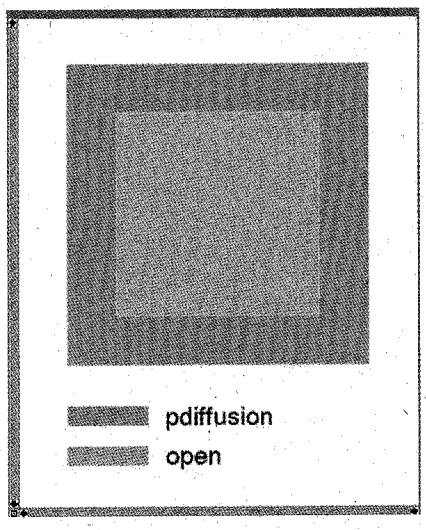
4. Top view of two openings similar to those shown in Fig. 3 but closer together. The pit is the largest rectangle formed by these openings. A suspended corner region results.



5. A top view of three rectangular openings in the shape of a "U." The pit is formed and a cantilever structure results.



6. The openings used for the pixel structure.



7. A test structure that includes the open tile with a surrounding p+ implant. This structure helps determine the etch rate of an etchant.

following four digitized areas: active area (CAA), contact (CCA), via (CVA), and glass (COG).

The "drc" section specifies the design rules for the "open"-to-"open" minimum spacing between distinct structures as 20 μm (assuming the chips are manufactured on a processing run where the feature size is 2.0 μm, which generally corresponds to a lambda of 1). If this design rule is violated, separate structures may inadvertently become connected after the etch. The minimum size of an open area has not yet been determined, but 5 μm (assuming a lambda of 1) has been used in a test structure similar to the one described in the examples section below. It may be difficult to obtain tighter than 5 μm processing control on the glass layer, a component of the open layer.

Designing Suspended Structures

To design layouts that realize suspended structures when standard CMOS chips are post-processed in an anisotropic etch, the designer must be aware of several special design considerations. Among them is the alignment of the design and the use of p+ boron doping to minimize undercutting. In this section, a brief overview of these considerations is presented, along with examples of a single cavity and multiple cavities that create suspended structures. Some physical explanations are included, and more details can be found in the references [10, 11, 13].

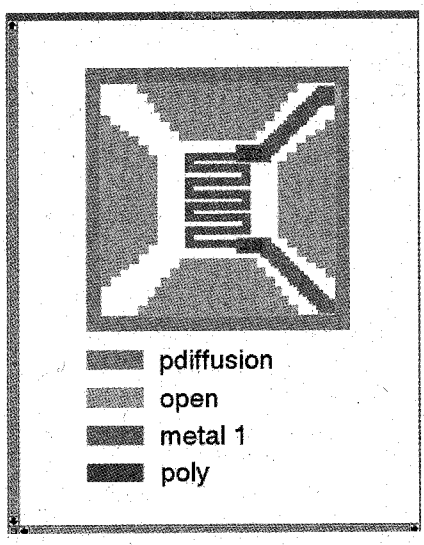
The etchant EDP was chosen for this work because it allows both SiO_2 and Al to be used as masking materials. This is important because the surface of CMOS chips are covered by SiO_2 for passivation and the bond pads are aluminum. Therefore, the only areas exposed to the etch are the open regions designed in the CAD layout. These are the factors that give rise to a maskless etch procedure for realizing the suspended structures in standard CMOS.

The first special design consideration is orientation and alignment of the design. In order to maintain control over the directions of the etch, designs must be aligned to lines corresponding to the intersection of the {111} crystalographic plane and the wafer-surface plane [14]. This is easily accomplished if one designs structures on the Cartesian coordinate grid system; that is, structures that are bounded by a perimeter that follows the x and y axes. The reason for this is that standard CMOS foundries use (100) silicon wafers for their process. The round wafers are supplied with a flat edge, or flat, that is oriented along this (110) intersection, and chips are aligned with respect to this water flat.

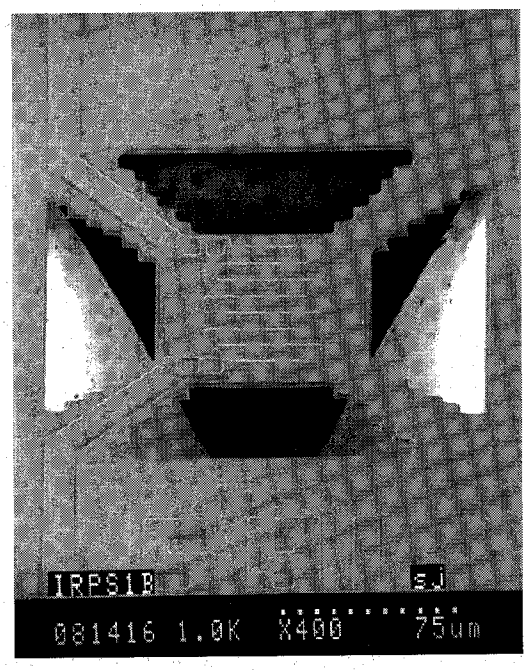
As an example, think of etching through a rectangular opening in the SiO_2 that is aligned to the x-y grid system of the CAD layout. Initially, the opening exposes the Si surface (Fig. 1a.) After some time in the anisotropic etch, a pit is formed with a flat bottom (Fig. 1b). The side walls of the pit are bounded by the {111} planes and form a 54.74° angle with respect to the silicon surface plane. Most of the etching occurs at the bottom of the pit. The four side walls finally intersect at a point, which halts the etching process (Fig. 1c).

The reason the side walls of the pit form a 54.74° angle with the surface is that the etch rate of the etchant varies with direction in the silicon crystal lattice; hence, the term "anisotropic" etch. It is of particular importance that the etch rate is significantly slower in the <111> direction than in the <100> direction. The etch-rate ratio for the EDP etchant used in this work is approximately 1:35 [11]. Therefore, the {111} planes function very nearly as etch stops. Note that there is some undercutting of the Si-SiO_2 surface in Fig. 1c because the etch rate in the {111} direction, although small, is not zero. This undercutting can be minimized by using a p+ boron implant at the perimeter of the open area. This p+ implant can be included in the design and provided by the foundry.

What is the effect of misaligning rectangular open area(s) to the x-y grid system? If a single open area is rotated by 45° from the x-y grid, after sufficient time in the etch solution the etched pit will be defined by the smallest rectangle that encompasses the open region and aligns to the x-y grid (Fig. 2a). In the case of two misaligned open areas that would have intersecting pit regions if the pits were formed individually, the pit



8. The design of a pixel structure used as an infrared point source.



9. A photomicrograph of the infrared-point-source pixel after etching. Credit: Sam Jones, NIST.

area is the smallest rectangular area formed by the two openings combined (Fig. 2b).

Things get interesting when we examine the effects of multiple aligned openings. Openings that are isolated and aligned lead to isolated pit regions (Fig. 3). Bring these openings together, and the pit is defined by the largest rectangle formed by the openings. If two such openings are brought together, a suspended corner region is produced (Fig. 4). In the standard foundry process, this suspended structure can contain layer(s) of polysilicon and aluminum encapsulated in glass (the standard foundry process may have multiple layers of polysilicon and aluminum). If three openings are brought together to form a "U", a cantilever structure results (Fig. 5). In this work the pixel structure shown in Fig. 6 is used.

Design Examples using Magic

Figure 7 shows a test structure that aids in determining an etchant's etch rate. This structure includes an open tile: the interior square surrounded by the p+ implant. Etch rate is determined by observing the change in depth versus time of the open area for various sizes of the structure shown in Fig. 7. The side walls in the open areas of the smaller structures will meet first, thus halting the rapid etch.

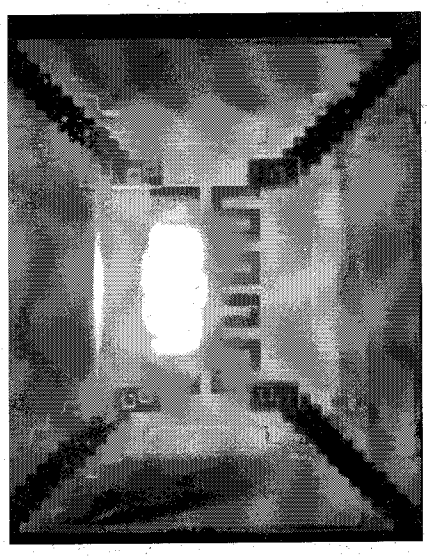
The CIF file for the digitized test structure of Fig. 7 was created by the "scm" technology file and is given in Table II. Note that MOSIS's familiar SCMOS CIF layers are being used for the open tile.

Figure 8 shows a micro-heater structure that is used as an infrared point source and an IR pixel for a thermal display. It was sent to MOSIS for fabrication as a 2.0-μm design. When the chips were received from MOSIS they were first dipped in a 2-percent buffered HCL solution for 10 seconds to strip away any native oxide in the open areas. The chips were then emersed in a gently stirred EDP solution at 100C in a reflux container for 2 1/2 hours (Fig. 9). (This is the step that creates the suspended structures.) The actual time spent in the EDP solution is a function of the device size. In general, one would like to minimize the time a device spends in the etch solution.

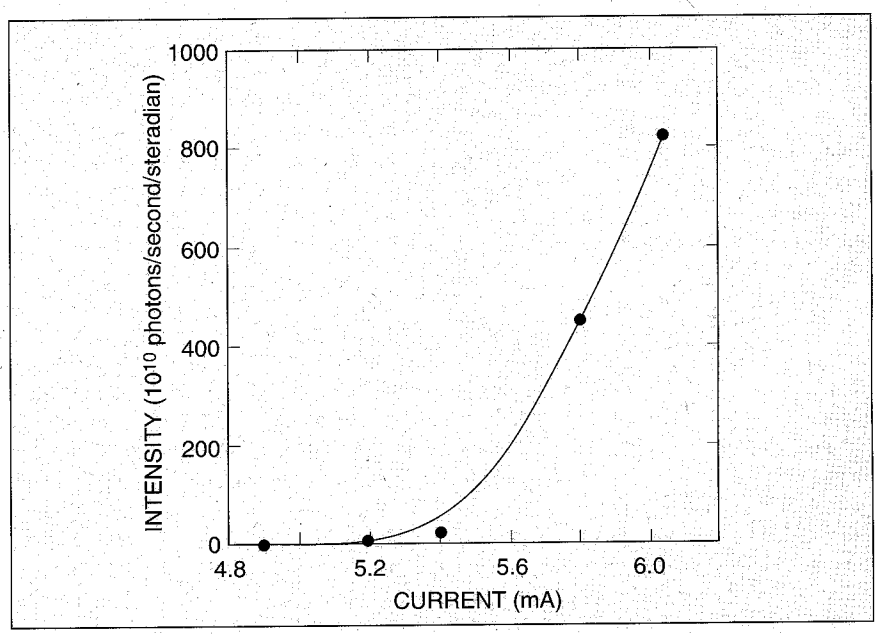
The thermally isolated resistor shown in Fig. 9 was brought to incandescence (Fig. 10) by applying 8 volts across the resistor, which caused a current flow of 3 mA. The low power of 24 mW can produce incandescence because heat is not absorbed by the underlying silicon substrate. The radiative intensity can be controlled by the drive current (Fig. 11). This device has possible applications in the area of dynamic thermal scene simulation [15].

Conclusions

The SCMOS technology file for Magic can be successfully modified to include the "open layer." This layer is the basic element needed to realize suspended mem-



10. The infrared point source operating at incandescence. Credit: M. Parameswaran, Simon Fraser University.



11. A plot of radiative intensity versus drive current for the infrared point source.

branes composed of the SiO_2, polysilicon, and aluminum layers inherent in a CMOS process. Devices that sense or produce movement based on the electro-thermo-mechanical properties of these layers can be designed and fabricated using commercial CMOS foundries through MOSIS.

The relatively low cost, high yield, and reliability of design and fabrication using the MOSIS service makes silicon micromachining possible for universities, government laboratories, and businesses.

Devices have been fabricated successfully with a lambda of 1. Further work must be done to validate the feasibility of smaller feature sizes. On-going work for the design of silicon micromachined structures in standard CMOS foundries includes further testing for the development of optimum design rules, including the minimum/maximum open size, the open-to-open spacing for separate structures and in the same structure to realize suspended structures, and the proximity of digital circuits. On-going work also includes studies for optimizing the design of supports for suspension and exploring an optimized device structure for thermal effects. Development of standard libraries for micromachined devices in standard CMOS processes will be available as applications are developed. Testing and characterization measurements will also be required. Finally, a more detailed understanding and modeling of the anisotropic etching of silicon is needed [16].

Acknowledgment

The authors would like to thank Wes Hansford and Vance Tyree from MOSIS for support in this work, and Don Novotny at NIST for help with the post-process etching procedure. We also acknowledge support from the Navy Advance Test Equipment/Metrology (ATE/M) Project at NOSC in San Diego and the Army Test Measurements and Diagnostic Equipment (TMDE) Activity at Redstone Arsenal, Alabama. **CD**

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Table II: CIF File for the Test Structure of Fig. 7

```
DS 1 1 2;
9 open50;
L CAA;
   B 22000 4000 -202600 4000;
   B 4000 14000 -211600 -5000;
   B 10000 10000 -202600 -5000;
   B 4000 14000 -193600 -5000;
   B 22000 4000 -202600 -14000;
L CVA;
   B 10000 10000 -202600 -5000;
L CCA;
   B 10000 10000 -202600 -5000;
L CSP;
   B 22800 4800 -202600 4000;
   B 4800 13200 -211600 -5000;
   B 4800 13200 -193600 -5000;
   B 22800 4800 -202600 -14000;
L COG;
   B 10000 10000 -202600 -5000;
DF;
C 1;
End
```

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Appendix
The Main Features of the Scalable CMOS Micromachine (SCM) Technology File

```
tech
    scm
end

planes
    oxide,ox
    metal2,m2
    metal1,m1
    active,diffusion,polysilicon,act
    well,w
    open
    labelb
end

types /* tiles */

    /* primary layers */

    well  bondpad
    metal2 pad
    oxide  glass
    metal2 metal2,m2,purple
    metal1 metal1,m1,blue
    active polysilicon,red,poly,p
    active ndiffusion,green,ndiff
    active pdiffusion,brown,pdiff
    active nndiff
    active ppdiff
    well  nwell,nw
    well  pwell,pw
    open  open

    open legend
    labelb legb,legend_background

   /* Contacts between interconnection layers
*/

    metal1 m2contact,m2c,via,v
    active polycontact,pcontact,pc
    active ndcontact,ndc
    active pdcontact,pdc
    active nwc,nwcontact
    active pwc,pwcontact

    /* Transistors */

    active ntransistor,nfet
    active ptransistor,pfet

end

contact /* contacts between planes */
    pad  metal2 metal1
    m2c  metal2 metal1
    pc  poly  metal1
    ndc  ndiff metal1
    pdc  pdiff metal1
    nwc  nndiff metal1
    pwc  ppdiff metal1
end

styles /* colors */
    styletype mos

    poly   1
    ndiff   2
    pdiff   4
    nfet   6
    nfet   7
    pfet   8
    pfet   9
    metal1 20
    metal2 21
    pc   1
    pc  20
    pc  32
    ndc   2
    ndc  20
    ndc  32
    pdc   4
    pdc  20
    pdc  32
    m2c  20
    m2c  21
    m2c  33
    pwc   5
    pwc  20
    pwc  32
    nwc   3
    nwc  20
    nwc  32
    ppdiff  5
    nndiff  3
    nwell  12
    pwell  13

/*  pad  20
    pad  21
*/
    pad  32

    glass  34

    open  33

    legend  1
    legb  32
    bondpad 32

    error_p 42
    error_s 42
    error_ps 42
end
```

```
compose /* to create structures in same plane
*/
    compose nfet poly ndiff
    compose pfet poly pdiff

    erase glass metal1 space
    erase glass metal2 space

end

#define allMetal2 m2,m2c/m2,pad/m2
#define                              allMetal1
m1,m2c/m1,pc/m1,ndc/m1,pdc/m1,pwc/m1,nwc/m1
,pad/m1
#define allPoly poly,pc/active,nfet,pfet
#define    allDiff0    pwc/active,nwc/ac-
tive,ppdiff,nndiff
#define allDiff allDiff0,ndiff,pdiff,ndc/ac-
tive,pdc/active,pfet,nfet
#define allNwell nwell,nwc/active
#define allPwell pwell,pwc/active

cifoutput

style lambda=1.0(gen)
    scalefactor 100
    layer CWN allNwell
    layer CWP allPwell
    layer CMS allMetal2
    layer CMF allMetal1
    layer CPG allPoly
    layer CAA allDiff,open
    layer CVA pad,m2c,open
    layer CCA ndc,pdc,nwc,pwc,open
    layer CCP pc
    layer CSN
 bloat-or ndiff,nfet,ndc/active * 200
 bloat-or nwc/active,nndiff * 200
 grow 100
 shrink 100
    layer CSP
 bloat-or pdiff,pfet,pdc/active * 200
 bloat-or pwc/active,ppdiff * 200
 grow 100
 shrink 100
    layer COG pad,glass,open
end

cifinput

style lambda=1.0(gen)
    scalefactor 100
    layer nw CWN
    layer pw CWP
    layer m2 CMS
    layer m1 CMF
    layer poly CPG
    layer pdiff CSP
    and CAA
      layer ndiff CSN
    and CAA
      layer nndiff CWN
    and CSN
    and CAA
      layer ppdiff CWP
    and CSP
    and CAA
      layer nfet CPG
    and CAA
    and CSN
      layer pfet CAA
    and CPG
    and CSP
      layer ndc CCA
    and CAA
    and CSN
    and CMF
      layer pdc CCA
    and CAA
    and CSP
    and CMF
      layer nwc CCA
    and CAA
    and CSN
    and CWN
    and CMF
      layer pwc CCA
    and CAA
    and CSP
    and CWP
    and CMF
      layer m2c CVA
    and CMS
    and CMF
      layer pc CCP
    and CPG
    and CMF
      layer pad CMF
    and CMS
    and CVA
    and COG
      layer glass COG
    and-not CVA
      layer open CAA
    and CCA
    and CVA
    and COG

end

drc
    spacing open open 20 touching_ok \
  "Open spacing must be at least 20 (Our rule
#0.1)"

end
```